AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (previously presented) A semiconductor integrated circuit comprising a nonvolatile memory enabling electric erase and write over a semiconductor substrate,

wherein said nonvolatile memory comprises a plurality of blocks each of which has a plurality of first bit lines, a plurality of second bit lines, a plurality of third bit lines and a plurality of first amplifiers,

wherein each of said first bit lines is coupled with an input terminal of a corresponding one of said first amplifiers,

wherein each of said second bit lines is coupled with an output terminal of a corresponding one of said first amplifiers, and

wherein each of said third bit lines is selectively coupled with a corresponding one of said first bit lines and is used for transferring data to be written into a memory cell.

2. (previously presented) The semiconductor integrated circuit according to claim 1,

wherein each of said first amplifiers is a differential amplifier having two input terminals and said output terminal, one input terminal is coupled to one of said first bit lines and the other input terminal is coupled to another of said first bit lines, and

wherein each of said first amplifiers is capable of using a signal inputted in one of said two input terminals as a reference signal to sense data.

3. (previously presented) The semiconductor integrated circuit according to claim 1, further comprising a plurality of second amplifiers,

wherein an input terminal of each of said second amplifiers is coupled to corresponding one of said second bit lines.

4. (previously presented) The semiconductor integrated circuit according to claim 3,

wherein each of said second amplifiers is a differential amplifier having two input terminals and an output terminal, one input terminal is coupled to one of

said second bit lines and the other input terminal is coupled to another of said second bit lines, and

wherein each of said second amplifiers is capable of using a signal inputted in one of said two input terminals as a reference signal to sense data.

5. (previously presented) The semiconductor integrated circuit according to claim 2, further comprising a first switch circuit,

wherein said first switch circuit is arranged between said first bit lines and said first amplifiers for selecting one of said first bit lines to be coupled with said one input terminal of said first amplifier.

6. (previously presented) The semiconductor integrated circuit according to claim 5, further comprising a second switch circuit,

wherein said second switch circuit is arranged between said first bit lines and said third bit lines for coupling said corresponding one of said first bit lines with one of said third bit lines.

7. (previously presented) The semiconductor integrated circuit according to claim 6, further comprising a plurality of third amplifiers each of which is coupled with a corresponding one of said third bit lines and is capable of sensing verify read data from a coupled third bit line.

8. (previously presented) The semiconductor integrated circuit according to claim 1,

wherein first power source wires are provided in parallel for every first amplifier, second power source wires wider than the first power source wires are provided in positions spaced from the first power source wires, and the first power source wires are coupled to the second power source wires by third power source wires laid in the first bit line direction.

9. (previously presented) The semiconductor integrated circuit according to claim 8, further comprising:

a plurality of third bit lines for write shared between said plurality of blocks in such a manner that one of the plurality of third bit lines is provided for every two first bit lines; and

said second switch circuit being capable of selectively coupling one third bit line to any one of the corresponding two first bit lines in each of said blocks.

10. (previously presented) The semiconductor integrated circuit according to claim 9,

wherein said third power source wires are arranged between every two adjacent first bit lines.

11. (previously presented) The semiconductor integrated circuit according to claim 6, further comprising:

a first address decoder being used in a read operation for selecting one of a plurality of word lines, ones of said first bit lines, said second switch circuit and ones of said first amplifiers; and

a second address decoder being used in a write operation for selecting one of said word lines and said second switch circuit.

12. (previously presented) The semiconductor integrated circuit according to claim 11,

wherein each of said first address decoder and said second address decoder includes address code logic performing address mapping so that said blocks, each of

which couples to one of said first amplifiers via said first bit lines therein, are arranged with non-consecutive addresses.

13. (currently amended) The semiconductor integrated circuit according to claim 12,

wherein in a read operation, the first address decoder holds an address decode signal and a select signal of the first bit line for each of said blocks corresponding to ~~the~~ a change of an address signal during ~~the~~ a number of cycles necessary for the read operation, and responds to the change of the address signal to operate ~~said~~ said first amplifiers with delay.

14. (currently amended) The semiconductor integrated circuit according to claim 12,

wherein in a read operation, the first address decoder selects, in parallel, word lines and first bit lines according to an address and ~~the~~ a next address, each of which is specified by address signals, drive controls the driving of the second bit line of ~~the~~ respective first amplifiers corresponding to said specified address and continuously drive controls corresponding to said next address.

15. (original) The semiconductor integrated circuit according to claim 12, further comprising a central processing unit capable of accessing said nonvolatile memory on said semiconductor substrate.

16. (currently amended) The semiconductor integrated circuit according to claim 15,

wherein one or more of said plurality of blocks are used as a data area, ~~the~~ a remaining number of said plurality of blocks are used as a management area, and said management area includes a storage area of a rewrite sequence control program for rewriting the data area,

wherein said central processing unit reads and executes the rewrite sequence control program from said storage area and enables rewrite control of the data area.

17. (currently amended) A semiconductor integrated circuit comprising: a nonvolatile memory enabling electric erase and write; and a central processing unit capable of accessing said nonvolatile memory on a semiconductor substrate,

wherein said nonvolatile memory comprises a hierarchal bit line structure including first bit lines specific to

each of a plurality of memory arrays, a plurality of second bit lines shared between the first bit lines of the plurality of memory arrays, and a plurality of sense amps arranged between said first bit lines and second bit lines, and ~~the~~ a number of said second bit lines is smaller than ~~the~~ a parallel write bit number to the memory array.

18. (original) The semiconductor integrated circuit according to claim 17, further comprising a third bit line for write shared between said plurality of memory arrays.

19. (currently amended) The semiconductor integrated circuit according to claim 18, further comprising a disconnect circuit capable of connecting and disconnecting ~~the~~ a corresponding first bit line for each of the memory arrays to/from the third bit line, wherein the disconnect circuit ~~controls dis-coupling the first bit line of the memory array to be read~~ effects said disconnecting in a read operation ~~from the third bit line~~.

20. (currently amended) A semiconductor integrated circuit comprising a nonvolatile memory enabling electric erase and write on a semiconductor substrate,

wherein said nonvolatile memory comprises a hierarchal bit line structure including first bit lines specific to each of a plurality of memory arrays, a second bit line shared between the first bit lines ~~of the plurality of memory arrays~~, and a sense amp selectively amplifying data read from each said first bit line to output the amplified data to the second bit line.

Claims 21-25 (canceled).